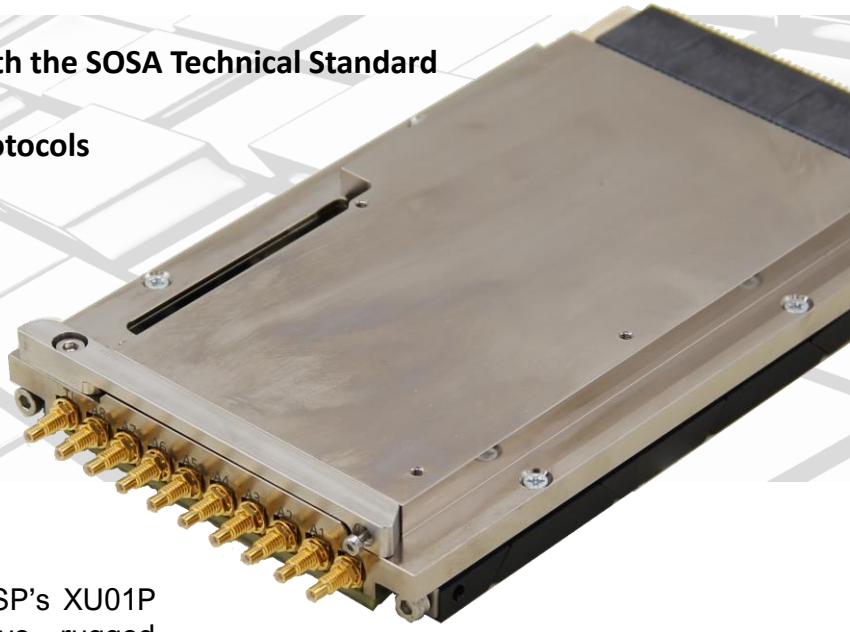
V3UADC01P Xilinx UltraScale 8CH ADC

Rugged mid-range FPGA data acquisition and processing for cost sensitive defence, aerospace and industrial programs

- **3U VPX Monolithic 8CH Digitizer aligned with the SOSA Technical Standard**
- **Xilinx® UltraScale™ FPGA processor**
- **Data & expansion planes for high-speed protocols**
- **Wide range of OpenVPX slot profiles**
- **Up to 8GB DDR4 ECC memory**
- **Analogue-to-Digital Convertor**
  - **8-channels 250Msps 14-bit ADC**
- **Air or conduction cooled**
- **Designed and made in the Netherlands**
- **Long-term Availability and Security Assured**



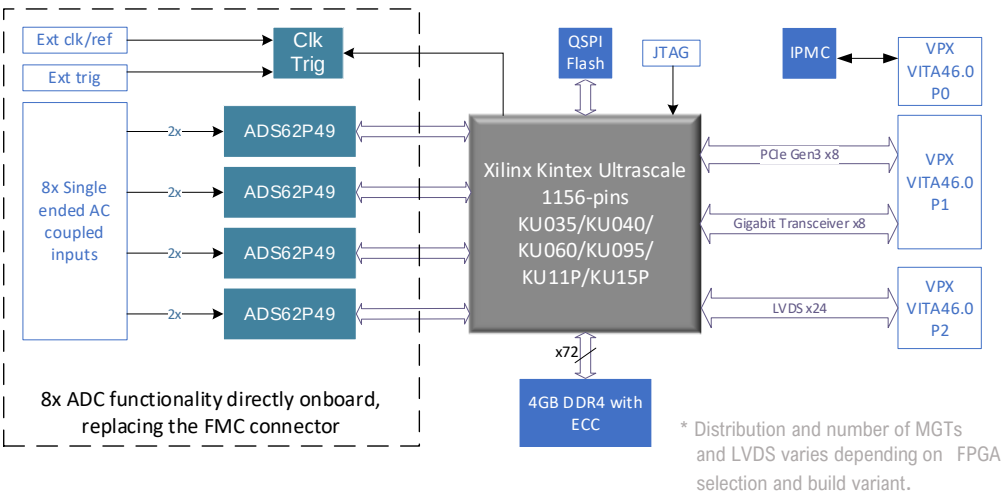
DESCRIPTION

The 3U V3UADC01P is a member of Hybrid DSP's XU01P 1156 Core Series of mid-range, cost effective, rugged processing boards based on the Xilinx Kintex UltraScale A1156 FPGA package, up to 8GB DDR4 and an ARM-based Board Management Controller (BMC).

The V3UADC01P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include eight ADC channels running at up to 250Msps with coax on either the front panel or optionally VITA 67 coax blind mate connectors on the backplane. The board supports external and internal trigger and clock sources.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the type of coax connectors, front panel design, cooling solution, reference firmware, and BMC.

The monolithic V3UADC01P is based on the V3UFMC01P and a customer's legacy FMC ADC module. Hybrid DSP's Modified-COTS optimized base XU01P design permitted a low-risk, rapid form-fit-function replacement of the existing modular solution leading to simplification of supply-chain, lifecycle management and serviceability, as well as a significant cost-saving across the program lifetime.



* Distribution and number of MGTs and LVDS varies depending on FPGA selection and build variant.

url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **Xilinx Kintex UltraScale™ A1156 FPGA XCKU035, XCKU040, XCKU060, XCKU095, XQKU040, XQKU060, XQKU095**
- **DDR4 4GB or 8GB with ECC**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (3U)
- **Up to 16 serial transceiver lanes on VPX P1 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 35 LVDS on VPX P2**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 67 Coaxial options**

Analogue Front-End
- **8-channels 250Msps 14-bit ADC**
- **ENOB 10.8 bit, SFDR 84dBc**

Mechanical
- **3U VPX COTS and Custom air- and conduction-cooled compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1” and 0.8”**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

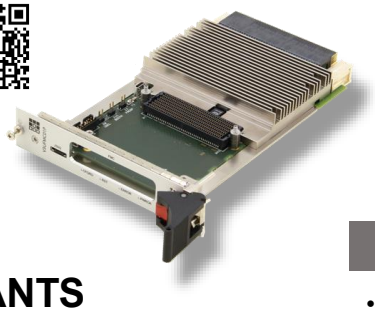
Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**

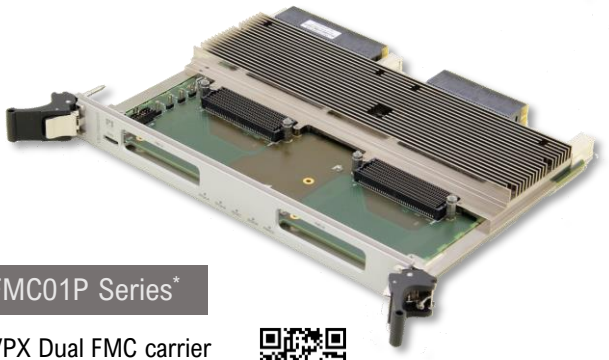
VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

RELATED PRODUCTS

V3UFMC01P Series*

- 3U VPX FMC Carrier
- Kintex UltraScale FPGA
- VITA 57.4 FMC+ Site



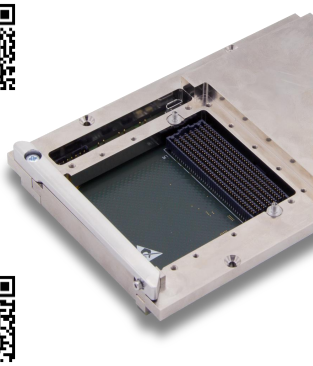


V6UFMC01P Series*

- 6U VPX Dual FMC carrier
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

V3UFMC02P Series*

- 3U VPX FMC Carrier
- Based on **V3UFMC01P**
- Kintex UltraScale+ FPGA



V3UFMC51P Series*

- 3U VPX FMC Carrier
- High-end Series
- Virtex UltraScale+ 2104
- Roadmap Product

SUPPORT AND VARIANTS

Hybrid DSP Systems supports her customers in the specification, design, production, integration and long-term product and life-cycle management of high-end rugged COTS and Modified-COTS 3U/6U VPX payload and I/O boards for VPX and OpenVPX based systems as well as those aligned with the SOSA Technical Standard.

Security of design and supply chain is increasingly important: the boards, firmware and software are designed and produced in the Netherlands. The Board Management Controller with VITA 46.11 IPMI is an in-house source available implementation.

The processes and IP used to design, produce and support her range of COTS products are fully modular and can be licensed on a flexible basis. Backed by discrete professional support and delivered and regularly updated in a transparent, traceable manner via private git repositories, the IP includes everything from complete board designs to source code and from mechanical files to documentation.

Contact Hybrid DSP to discuss how we can accelerate your next development.

1. SOSA and logo design and The Open Group Certification Mark™ are trademarks of The Open Group in the United States and other countries.
2. The VPX logo and related marks are trademarks of VITA
3. Hybrid DSP is a preferred FPGA partner to Mercury Systems
** Products and solutions were developed in alignment with the SOSA™ Technical Standard*

url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands