V3UFMC51P Virtex UltraScale+ FMC+ Carrier

**Rugged high-end FPGA processing for demanding defence, aerospace and industrial programs**

- 3U VPX FPGA FMC Carrier aligned with the SOSA Technical Standard
- AMD® UltraScale+™ FPGA processor
- Data & expansion planes for high-speed protocols
- Wide range of OpenVPX slot profiles
- Up to 16GB DDR4 ECC memory
- Air or conduction cooled
- Designed and made in the Netherlands
- Long-term Availability and Security Assured
- VITA 57.4 FMC+ mezzanine site for I/O module

DESCRIPTION

The 3U V3UFMC51P is a member of Hybrid DSP's XU51P Series of high-end, rugged processing boards based on the AMD Virtex UltraScale+ A2104 FPGA package, up to 16GB DDR4 and an ARM-based Board Management Controller (BMC). The V3UFMC51P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include an FMC+ site to support mezzanine cards with I/O routing to either the front panel or optionally VITA 66/67 optical/coax blind mate connectors on the backplane.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the front-panel, cooling solution, reference firmware, and BMC. Furthermore, the PCB layout and stack-up allows for a viable low-risk route for more complex technical and commercial requirements including modular-to-monolithic.
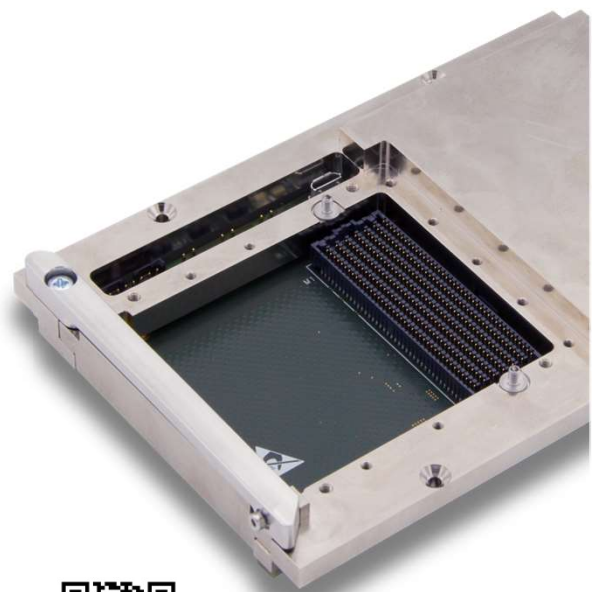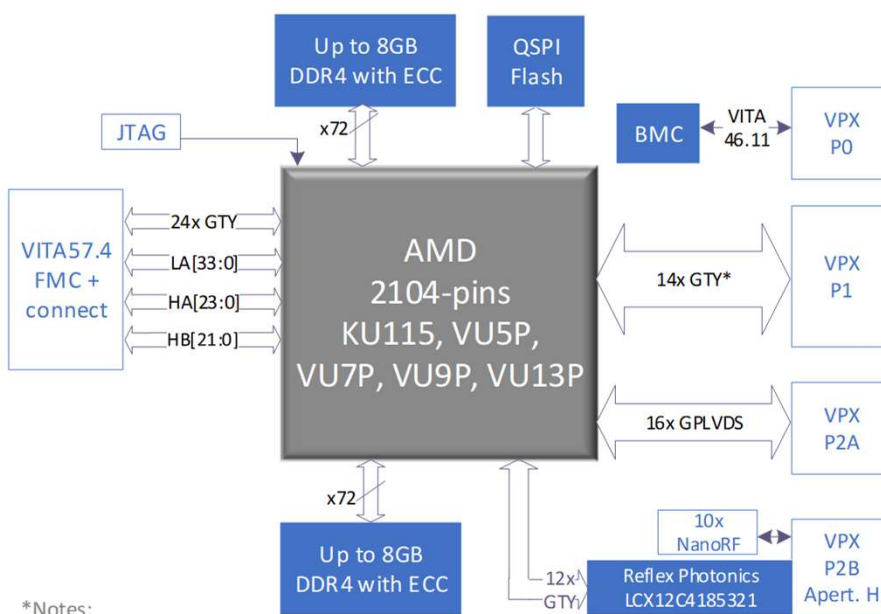
*Notes:
- VPX P1.9 – P1.16 supports PCIe Gen3 2x4 or 1x8
- In alignment with SOSA PIC Profiles:
  MOD3-PAY-1F1U1S1S1U1U4F1J-16.6.13-3
  MOD3-PAY-1F1U1S1S1U1U4F1J-16.6.13-5

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VPX™   SOSA Sensor Open Systems Architecture   **PRELIMINARY DATASHEET - CONFIDENTIAL**

Kanaalpark 157
2321JW Leiden
The Netherlands

TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **AMD Virtex UltraScale+™ A2104 FPGA VU5P, VU7P, VU9P, V13P**
- **Dual DDR4 4GB or 8GB with ECC**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (3U)
- **Up to 16 serial transceiver lanes on VPX P1 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 16 LVDS on VPX P2A**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 66/67 Optical and Coaxial options**

Front Panel I/O
- **FMC+ site per VITA 57.4**
- **Extended component free region**

Mechanical
- **3U VPX COTS and Custom air- and conduction-cooled (FMC+) compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1" and 0.8"**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**
- **VITA 57.4**

VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

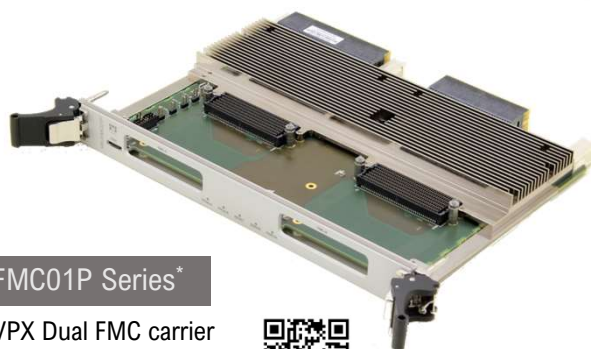## RELATED PRODUCTS

V3UADC01P Series*
- 3U VPX Monolithic ADC
- Based on **V3UFMC01P** Design
- 8-channel 250Msps ADC
- Internal and external clock

V6UFMC01P Series*
- 6U VPX Dual FMC carrier
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

SUPPORT AND VARIANTS

Hybrid DSP Systems supports her customers in the specification, design, production, integration and long-term product and life-cycle management of high-end rugged COTS and Modified-COTS 3U/6U VPX payload and I/O boards for VPX and OpenVPX based systems as well as those aligned with the SOSA Technical Standard.

Security of design and supply chain is increasingly important: the boards, firmware and software are designed and produced in the Netherlands. The Board Management Controller with VITA 46.11 IPMI is an in-house source available implementation.

The processes and IP used to design, produce and support her range of COTS products are fully modular and can be licensed on a flexible basis. Backed by discrete professional support and delivered and regularly updated in a transparent, traceable manner via private git repositories, the IP includes everything from complete board designs to source code and from mechanical files to documentation.

Contact Hybrid DSP to discuss how we can accelerate your next development.

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