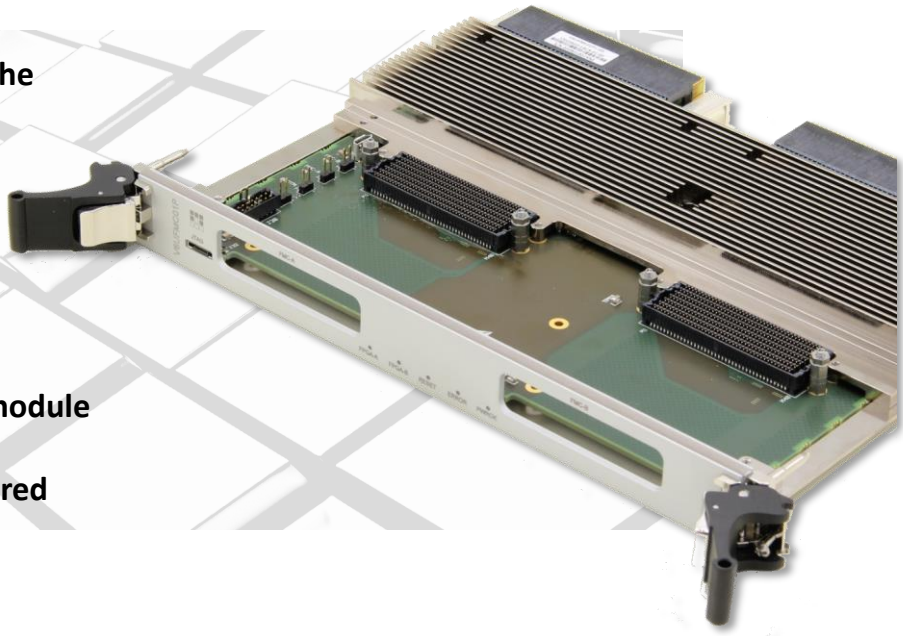
V6UFMC02P Xilinx UltraScale+ FMC+ Carrier

Rugged mid-range FPGA processing for cost sensitive defence, aerospace and industrial programs

- **6U VPX FPGA FMC Carrier aligned with the SOSA Technical Standard**
- **Data & expansion planes for high-speed protocols**
- **Xilinx® UltraScale+™ FPGA processors**
- **Wide range of OpenVPX slot profiles**
- **Air or conduction cooled**
- **Up to 8GB DDR4 ECC memory per FPGA**
- **VITA 57.4 FMC+ mezzanine site for I/O module**
- **Designed and made in the Netherlands**
- **Long-term Availability and Security Assured**

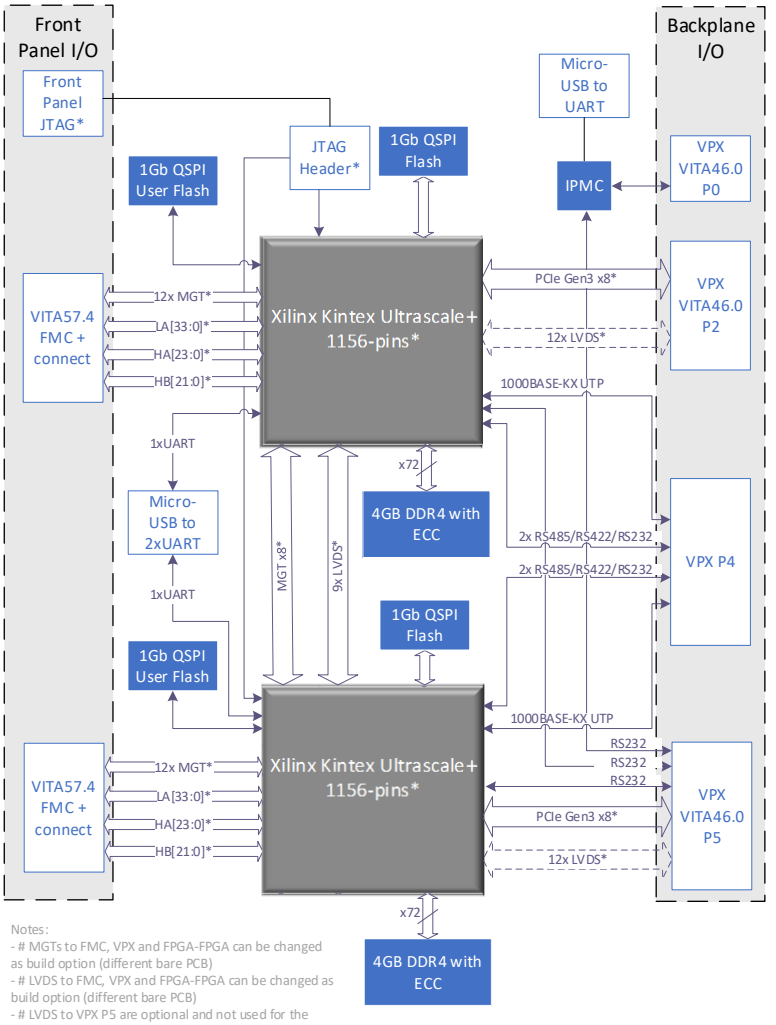


DESCRIPTION

The 6U V6UFMC02P is a member of Hybrid DSP's XU02P 1156 Core Series of mid-range, cost effective, rugged processing boards based on the Xilinx Kintex UltraScale+ A1156 FPGA package, up to 8GB DDR4 per FPGA and an ARM-based Board Management Controller (BMC).

The V6UFMC02P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include two FMC+ sites to support mezzanine cards with I/O routing to either the front panel or optionally VITA 66/67 optical/coax blind mate connectors on the backplane.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the front-panel, cooling solution, reference firmware, and BMC. Furthermore, the PCB layout and stack-up allows for a viable low-risk route for more complex technical and commercial requirements including modular-to-monolithic.



Notes:
- # MGTs to FMC, VPX and FPGA-FPGA can be changed as build option (different bare PCB)
- # LVDS to FMC, VPX and FPGA-FPGA can be changed as build option (different bare PCB)
- # LVDS to VPX P5 are optional and not used for the first project
- Compatible with SOSA MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H- 12.6.4- 1
- KU060 is designed for, however KU040, KU11P and KU15P FPGAs could be permitted as build option
- Front panel JTAG and on-board JTAG header are both accessible but operate mutually exclusive

* V6UFMC02P**1** shown above
V6UFMC02P**2** has MGT x4 inter-FPGA and additional MGT x4 to P2 and P5

url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **Xilinx Kintex UltraScale+™ A1156 FPGA XCKU11P, XCKU15P (Dual)**
- **DDR4 4GB or 8GB with ECC (per FPGA)**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (6U)
- **Up to 12 serial transceiver lanes on VPX P2 and P5 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 12 LVDS on VPX P2 and P5**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 66/67 Optical and Coaxial options**

Front Panel I/O
- **Two FMC+ sites per VITA 57.4**
- **Extended component free region**

Mechanical
- **6U VPX COTS and Custom air- and conduction-cooled (FMC+) compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1" and 0.8"**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**
- **VITA 57.4**

VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

RELATED PRODUCTS

V3UADC01P Series*

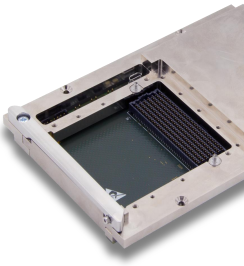
- 3U VPX Monolithic ADC
- Based on **V3UFMC01P** Design
- 8-channel 250Msps ADC
- Internal and external clock

V6UFMC01P Series*

- 6U VPX Dual FMC carrier
- Kintex UltraScale FPGA
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

V3UFMC01P Series*

- 3U VPX FMC Carrier
- Kintex UltraScale FPGA
- VITA 57.4 FMC+ Site



V3UFMC02P Series*

- 3U VPX FMC Carrier
- Based on **V3UFMC01P**
- Kintex UltraScale+ FPGA

V3UFMC51P Series*

- 3U VPX FMC Carrier
- High-end Series
- Virtex UltraScale+ 2104
- Roadmap Product

SUPPORT AND VARIANTS

Hybrid DSP Systems supports her customers in the specification, design, production, integration and long-term product and life-cycle management of high-end rugged COTS and Modified-COTS 3U/6U VPX payload and I/O boards for VPX and OpenVPX based systems as well as those aligned with the SOSA Technical Standard.

Security of design and supply chain is increasingly important: the boards, firmware and software are designed and produced in the Netherlands. The Board Management Controller with VITA 46.11 IPMI is an in-house source available implementation.

The processes and IP used to design, produce and support her range of COTS products are fully modular and can be licensed on a flexible basis. Backed by discrete professional support and delivered and regularly updated in a transparent, traceable manner via private git repositories, the IP includes everything from complete board designs to source code and from mechanical files to documentation.

Contact Hybrid DSP to discuss how we can accelerate your next development.

1. SOSA and logo design and The Open Group Certification Mark™ are trademarks of The Open Group in the United States and other countries.
2. The VPX logo and related marks are trademarks of VITA
3. Hybrid DSP is a preferred FPGA partner to Mercury Systems
** Products and solutions were developed in alignment with the SOSA™ Technical Standard*

url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands