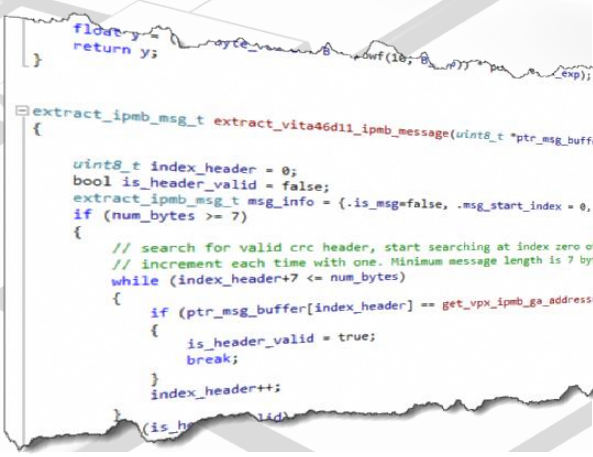
Hybrid DSP
Sensor Processing Solutions

VITA 46.11 Tier 3 IPMC

A readily maintainable and customizable BMC implementation with VITA 46.11 Tier 3 support for 3rd party board developments

- **VITA 46.11-2022 Tier 3 compliant IPMC software core**
- **Up to Tier 3 in alignment with SOSA Technical Standard**
- **Redundant IPMB interface**
- **Lightweight bare-metal C implementation, portable to RTOS**
- **Source code available**
- **Developed inhouse by Hybrid DSP in the Netherlands**
- **SDR and FRU compiler utilities**
- **Reference designs for easy customer integration**
- **VPX plug-in card BMC reference schematics on request**
- **Extensive documentation including Quick Start Guides**
- **Deliverables through GIT or a secured file transfer**



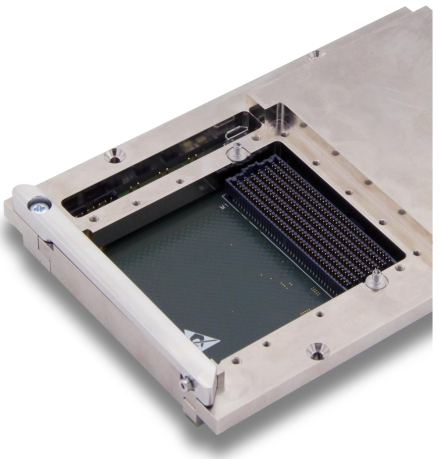
DESCRIPTION

The VITA 46.11-2022 software IP core implements all requirements defined for a Tier 3 IPMC. Typical target platforms of this software core are OpenVPX and SOSA aligned payload modules which interface to a Chassis Manager through the IPMB interfaces on the backplane.

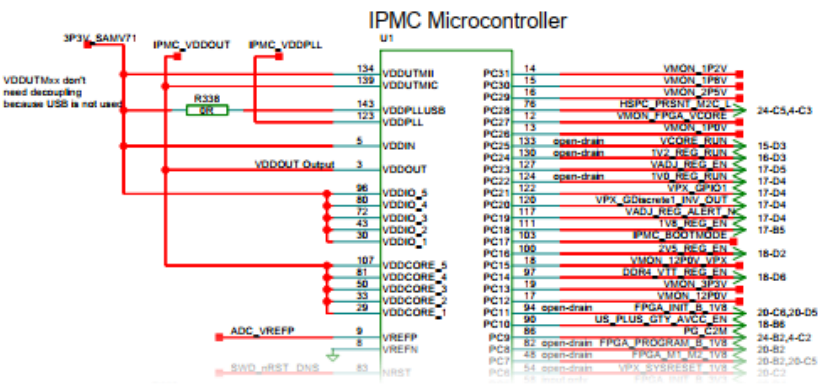
The bare-metal C implementation is lightweight and supports various microcontroller architectures such as ARM and RISC-V. Functions that make use of dedicated microcontroller peripherals are provided as part of reference designs, for example the I2C controller of the Microchip SAMV71 or the PolarFire® RISC-V SoC. Other microcontroller designs can be made available on request.

The IP core is delivered with an FRU and an SDR compiler utility. The SDR compiler takes sensor values and thresholds provided by the customer using the delivered SDR excel template. It generates required SDR data to be uploaded to the flash of the IPMC. Different output formats are available supporting standard file formats such as .hex and .bin, suitable for automated programming during board production.

Hybrid DSP provides support with integration or can fully implement customers board management and IPMC functionality.



SOSA™ Aligned reference design target platform: Hybrid DSP V3UFMC01Px Series



Reference design target platform: PolarFire® RISC-V SoC FPGA Icicle Kit [3]

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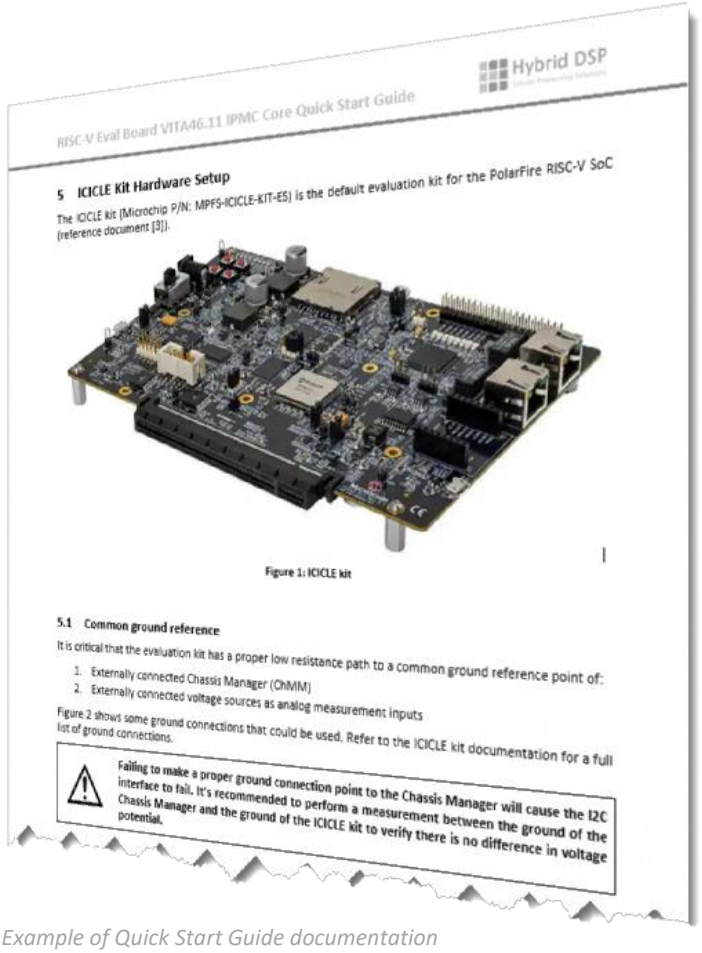
VITA 46.11 IPMC IP core and board management

DELIVERABLES

- VITA 46.11 IPMC source code
- Reference design
- SDR converter utility with templates
- FRU compiler with templates
- Documentation
- Provided as archive via secured file transfer, or customer facing private GIT repository for optimized version control (Clone, Fetch, Pull, Push)


RISC-V Eval Board VITA46.11 IPMC Core Quick Start Guide

5 ICICLE Kit Hardware Setup

The ICICLE kit (Microchip P/N: MPFS-ICICLE-KIT-ES) is the default evaluation kit for the PolarFire RISC-V SoC (reference document [3]).

Figure 1: ICICLE kit

5.1 Common ground reference

It is critical that the evaluation kit has a proper low resistance path to a common ground reference point of:

1. Externally connected Chassis Manager (ChMM)
2. Externally connected voltage sources as analog measurement inputs

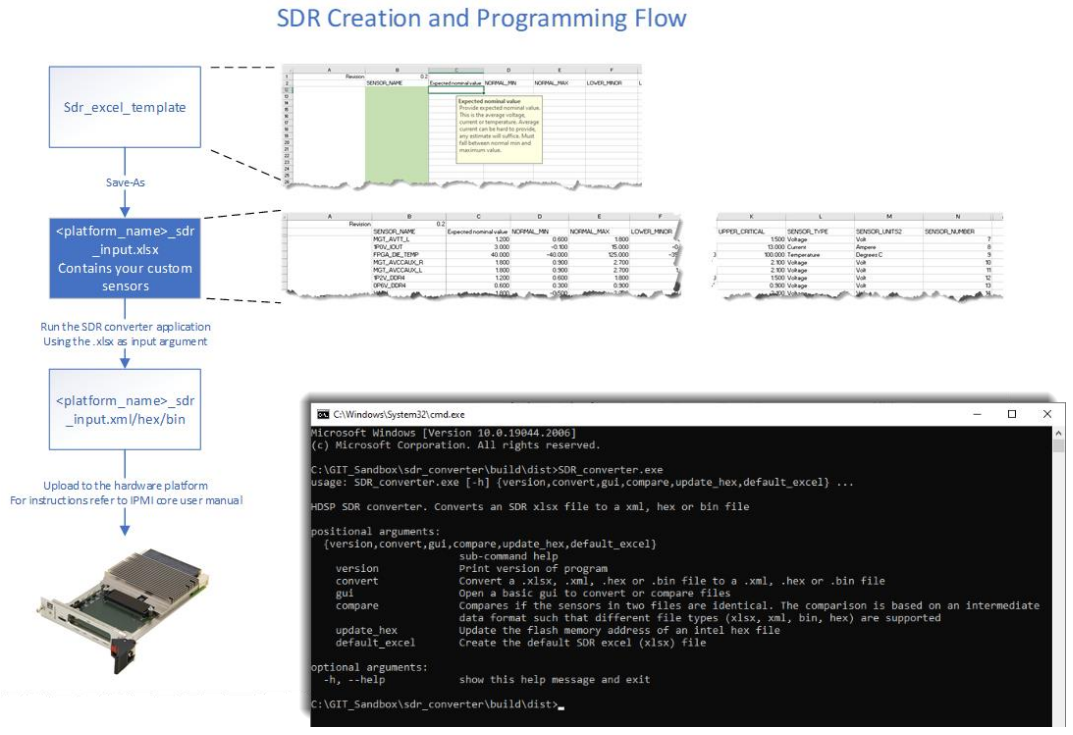
Figure 2 shows some ground connections that could be used. Refer to the ICICLE kit documentation for a full list of ground connections.

Failing to make a proper ground connection point to the Chassis Manager will cause the I2C interface to fail. It's recommended to perform a measurement between the ground of the Chassis Manager and the ground of the ICICLE kit to verify there is no difference in voltage potential.

Example of Quick Start Guide documentation

REFERENCE DESIGNS

- Default reference designs available for:
  - Microchip ATSAMV71-XULT, ARM
  - Microchip MPFS-ICICLE-KIT-ES, RISC-V
- Command Line Interface (CLI) through UART
- Redundant IPMB connection to Chassis Manager
- Chassis Manager to be provided by customer
- GA and NVMRO pin settings can be configured through CLI
- Threshold sensor values can be emulated through CLI to test event generation
- Quick Start Guide providing instructions to connect to Chassis Manager and get started with the software
- Ipmitool docker image with example use cases
- Custom BMC and IPMI reference and production designs available on request



Instructions embedded in SDR .xlsx template

SDR AND FRU UTILITIES

- SDR Spreadsheet .xlsx template permits addition of custom sensors without in-depth VITA 46.11 knowledge
- FRU .xml template to generate the minimum FRU data required by VITA 46.11
- Command line SDR and FRU converter generating .bin or Intel .hex files that can be uploaded through the standard IDE programming interfaces or a customer specific interface
- SDR and FRU compilers delivered as Windows Executables

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